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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/932,330	08/17/2001	Jon M. Huppenthal	SRC012	4801

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EXAMINER	
SORRELL, ERON J	
ART UNIT	**PAPER NUMBER**
2182	

DATE MAILED: 12/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/932,330	HUPPENTHAL ET AL.	
	Examiner	Art Unit	
	Eron J. Sorrell	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 9/21/05 has been entered.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is

shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1,3,4,9,10,11,13, and 23 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1,3,4,7,10,13,17,18, and 20 of copending Application No. 10/869,199. Although the conflicting claims are not identical, they are not patentably distinct from each other because the claims of the instant application recite limitations using the term "processor," while the claims of application 10/869,199 use the term "dense logic device" to describe the same functional unit. The independent claims of the instant application also recite the limitation of a processor element associated with a memory module slot, while the claims of application 10/869,199 recite a direct execution logic element coupled to an adapter port that is associated with a memory module slot to describe the same structure. Finally, the independent claims of the instant application require a peripheral bus slot coupled to a peripheral bus. The same limitation can be found in dependent claims of application 10/869,199.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 5,6,17, and 18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Claims 5,6,17, and 18 contain the trademark/trade name "RIMM". Where a trademark or trade name is used in a claim as a limitation to identify or describe a particular material or product, the claim does not comply with the requirements of 35 U.S.C. 112, second paragraph. See *Ex parte Simpson*, 218 USPQ 1020 (Bd. App. 1982). The claim scope is uncertain since the trademark or trade name cannot be used properly to identify any particular material or product. A trademark or trade name is used to identify a source of goods, and not the goods

themselves. Thus, a trademark or trade name does not identify or describe the goods associated with the trademark or trade name. In the present case, the trademark/trade name is used to identify/describe a memory module and, accordingly, the identification/description is indefinite.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-4,7-10,12-16, and 19-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Foster (U.S. Patent No. 6,052,134) in view of O'Sullivan (U.S. Patent No. 4,972,457).

6. Referring to claim 1, Foster teaches a computer system (see figure 1) comprising:

at least one processor (see item 12 of figure 1);

a controller (see item 14 in figure 2) for coupling the at least one processor to a peripheral bus control block (see item

28 in figure 1 and a memory bus (see bus coupling item 14 to item 18 in figure 1);

at least one peripheral bus slot coupled to the peripheral bus control block by a peripheral bus (see item 30a in figure 1 and lines 14-25 of column 6)

at least one memory module slot coupled to the memory module bus (see lines 30-55 of column 5).

Foster fails to teach the system further comprises a processor element associated with the at least one memory module slot for providing a data connection to an external device connected thereto.

O'Sullivan teaches a computer system comprising the above limitations (see item 70 in figure 4 and lines 50-59 of column 5 and lines 7-41 of column 7), and suggests the processor element (hybrid communications control unit), can be located in any available memory expansion slot within the computer.

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Foster with the above teachings of O'Sullivan. One of ordinary skill in the art would have been motivated to make such modification in order to add an adapter using an existing available slot without making any hardware changes in the

computer or purchasing additional equipment as suggested by O'Sullivan.

7. Referring to claim 13, Foster teaches a computer system (see figure 1) comprising:

at least one processor (see item 12 of figure 1);

a controller (see item 14 in figure 2) for coupling the at least one processor to a graphic bus control block (see item 20 in figure 1 and a memory bus (see bus coupling item 14 to item 18 in figure 1);

at least one graphics bus connection coupled to the graphics bus control block by a peripheral bus (see item 24 in figure 1 and paragraph bridging columns 5 and 6)

at least one memory module slot coupled to the memory module bus (see lines 30-55 of column 5).

Foster fails to teach the system further comprises a processor element associated with the at least one memory module slot for providing a data connection to an external device connected thereto.

O'Sullivan teaches a computer system comprising the above limitations (see item 70 in figure 4 and lines 50-59 of column 5 and lines 7-41 of column 7), and suggests the processor element

(hybrid communications control unit), can be located in any available memory expansion slot within the computer.

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Foster with the above teachings of O'Sullivan. One of ordinary skill in the art would have been motivated to make such modification in order to add an adapter using an existing available slot without making any hardware changes in the computer or purchasing additional equipment as suggested by O'Sullivan.

8. Referring to claims 2 and 14, O'Sullivan teaches a control connection to the peripheral port (see bus coupling item 70 to item 78 in figure 4) for indicating to the at least one processor an arrival of data on the data connection to the processor element (see lines 1-18 of column 6).

9. Referring to claims 3 and 15, Foster teaches memory module bus comprises a DIMM bus (see paragraph bridging columns 6 and 7; Note DIMMs have a 64-bit width and Foster discloses the memory banks disclosed have a 64-bit width).

10. Referring to claims 4 and 16, O'Sullivan teaches the processor element comprises a DIMM physical format for retention within one of the DIMM memory module slots.

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Foster with the above teachings of O'Sullivan. One of ordinary skill in the art would have been motivated to make such modification in order to add an adapter using an existing available slot without making any hardware changes in the computer or purchasing additional equipment as suggested by O'Sullivan.

11. Referring to claims 7 and 19, O'Sullivan teaches the external device comprises one of another computer system, switch or network (see item 40 in figure 4).

12. Referring to claim 8, Foster teaches the peripheral bus comprises a PCI bus (see item labeled PCI bus in figure 1).

13. Referring to claims 9,10,21, and 22 O'Sullivan teaches the processor element is operative data received from said controller on said memory bus and is operative alter data

received from an external source prior to placing altered data said memory bus (see lines 3-12 of column 4).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Foster with the above teachings of O'Sullivan in order for the data to be in the proper format/protocol for sending and receiving data.

14. Referring to claims 12 and 23, Foster the at least one processor comprises a plurality of processors (see lines 13-36 of column 1).

15. Referring to claim 20 and 24, Foster teaches the graphics bus comprises an AGP bus (see bus connecting items 14 and 20 in figure 1).

16. Claims 5,6,17,18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Foster in view of O'Sullivan as applied to claims 1 and 34 above, and further in view of Tetrick (U.S. patent No. 6,598,199).

17. Referring to claims 5,6,17,18 the combination of Foster and O'Sullivan fails to teach the memory module slots comprise RIMM

memory module slots and the adapter port comprises a RIMM physical format for retention within one of said RIMM memory module slots.

Tetrick teaches RIMMs are substantially similar to DIMMs, but use RDRAM chips which have faster access times than other DRAM or SDRAM chips (see lines 40-54 of column 2).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the combination of Foster and O'Sullivan with the above teachings of Tetrick in order to use a faster memory as suggested by Tetrick.

18. Claims 11 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Foster in view of O'Sullivan as applied to claims 1 and 13 above, and further in view of Chiles et al. (U.S. Patent No. 6,581,157).

19. Referring to claims 11 and 23 the combination of Foster and O'Sullivan fails to teach the processor element further comprises at least one field programmable gate array configurable to perform an identified algorithm on and operand provided thereto by said processor element.

Chiles teaches the above limitation (see item labeled 256 in figure 3 and paragraph bridging columns 8 and 9).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the combination of Foster and O'Sullivan with the teachings of Chiles. One of ordinary skill would have been motivated to make such modification in order to upgrade the adapter port without purchasing a new one.

20. Claims 25-28,31-34 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Foster in view of O'Sullivan and further in view of Whittaker et al. (U.S. Patent No. 5,889,959 hereinafter "Whittaker").

21. Referring to claim 25, Foster teaches a computer system (see figure 1) comprising:

at least one processor (see item 12 of figure 1);

a controller (see item 14 in figure 2) for coupling the at least one processor to a memory bus (see bus coupling item 14 to item 18 in figure 1);

at least one memory module slot coupled to the memory module bus (see lines 30-55 of column 5).

Foster fails to teach the system further comprises a controller for coupling the processor with a maintenance control block and a processor element associated with the at least one

memory module slot for providing a data connection to an external device connected thereto.

O'Sullivan teaches a computer system comprising and a processor element associated with the at least one memory module slot for providing a data connection to an external device connected thereto (see item 70 in figure 4 and lines 50-59 of column 5 and lines 7-41 of column 7), and suggests the processor element (hybrid communications control unit), can be located in any available memory expansion slot within the computer.

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Foster with the above teachings of O'Sullivan. One of ordinary skill in the art would have been motivated to make such modification in order to add an adapter using an existing available slot without making any hardware changes in the computer or purchasing additional equipment as suggested by O'Sullivan.

The combination of Foster and O'Sullivan fails to teach the control block comprises systems maintenance control block, wherein the systems maintenance control block provides control information to the processor element.

Whittaker teaches a control block comprising a systems maintenance control block, wherein the systems maintenance

control block provides control information processor element (see lines 42-49 of column 4).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the combination of Foster and O'Sullivan with the above teachings of Whittaker. One of ordinary skill in the art would have been motivated to make such modification in order to provide diagnostic functions to all of the modules in the system as suggested by Whittaker (see lines 30-43 of column 1).

22. Referring to claim 26, O'Sullivan teaches a control connection to the peripheral port (see bus coupling item 70 to item 78 in figure 4) for indicating to the at least one processor an arrival of data on the data connection to the processor element (see lines 1-18 of column 6).

23. Referring to claim 27, Foster teaches memory module bus comprises a DIMM bus (see paragraph bridging columns 6 and 7; Note DIMMs have a 64-bit width and Foster discloses the memory banks disclosed have a 64-bit width).

24. Referring to claims 28, O'Sullivan teaches the processor element comprises a DIMM physical format for retention within one of the DIMM memory module slots.

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Foster with the above teachings of O'Sullivan. One of ordinary skill in the art would have been motivated to make such modification in order to add an adapter using an existing available slot without making any hardware changes in the computer or purchasing additional equipment as suggested by O'Sullivan.

25. Referring to claims 31, O'Sullivan teaches the external device comprises one of another computer system, switch or network (see item 40 in figure 4).

26. Referring to claim 32, Whittaker teaches the system maintenance bus comprises a SM bus (see item 12B in figure 2).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the combination of Foster and O'Sullivan for the same reasons as outlined in the rejection of claim 25, supra.

27. Referring to claims 33 and 34 O'Sullivan teaches the processor element is operative data received from said controller on said memory bus and is operative alter data received from an external source prior to placing altered data said memory bus (see lines 3-12 of column 4).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Foster with the above teachings of O'Sullivan in order for the data to be in the proper format/protocol for sending and receiving data.

28. Referring to claims 36, Foster the at least one processor comprises a plurality of processors (see lines 13-36 of column 1).

29. Claims 29 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Foster in view of O'Sullivan as applied to claims 25 above, and further in view of Tetrick (U.S. Patent No. 6,598,199).

30. Referring to claims 29 and 30 the combination of Foster and O'Sullivan fails to teach the memory module slots comprise RIMM memory module slots and the adapter port comprises a RIMM

physical format for retention within one of said RIMM memory module slots.

Tetrick teaches RIMMs are substantially similar to DIMMs, but use RDRAM chips which have faster access times than other DRAM or SDRAM chips (see lines 40-54 of column 2).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the combination of Foster and O'Sullivan with the above teachings of Tetrick in order to use a faster memory as suggested by Tetrick.

31. Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over Foster in view of O'Sullivan and further in view of Whittaker as applied to claim 25 above, and further in view of Chiles et al. (U.S. Patent No. 6,581,157).

32. Referring to claims 36 the combination of Foster, O'Sullivan, and Whittaker fails to teach the processor element further comprises at least one field programmable gate array configurable to perform an identified algorithm on and operand provided thereto by said processor element.

Chiles teaches the above limitation (see item labeled 256 in figure 3 and paragraph bridging columns 8 and 9).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the combination of Foster and O'Sullivan with the teachings of Chiles. One of ordinary skill would have been motivated to make such modification in order to upgrade the adapter port without purchasing a new one.

Response to Arguments

33. Applicant's arguments with respect to claims 1,13, and 25 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eron J. Sorrell whose telephone number is 571 272-4160. The examiner can normally be reached on Monday-Friday 8:00AM - 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on 571-272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EJS
December 5, 2005

KIM HUYNH
PRIMARY EXAMINER
12/7/05